WHAT IS CLAIMED IS:

1. A non-volatile memory array structure, comprising:

a plurality of first transistors, serving for memory function, arranged to have a plurality of columns and a plurality of first rows, wherein the first transistors in each column are coupled in series at source/drain regions, and adjacent two of the columns are grouped into a memory group using a common bit line, and gate electrodes of the first transistors in the same first row are coupled with a first sequence word line; and

a plurality of second transistors, serving for memory function, wherein each of the second transistors, in commonly used source/drain regions, is coupled between two columns of the memory group and is adjacent to each of the first rows, so that the second transistors form a plurality of second rows, wherein gate electrodes of the second transistors in the same second row are coupled to a second sequence word line.

2. The non-volatile memory array structure of claim 1, wherein the first sequence word line is an even number word line and the second sequence word line is an odd number word line.

3. The non-volatile memory array structure of claim 1, wherein the first sequence word line intervenes with the second sequence word line.

4. The non-volatile memory array structure of claim 1, each column of the memory group further comprises an upper switching unit coupled between the bit line and the column, and a lower switching unit coupled between the bit line and a ground terminal, so that the switching units associated with the bit lines and the word lines is used to selected a desired flow path in the memory group.

5. The non-volatile memory array structure of claim 4, wherein each of the switching units includes a MOS transistor.

6. An accessing operation method for the non-volatile memory device as recited in claim 4, comprising performing a reading operation to read a content stored in a selected first transistor of the first transistors, wherein the reading operation comprising:

selecting a bit line with respect to the selected memory group;

setting a corresponding one of the first sequence word line, which has the selected first transistor, by a constant voltage;

setting the other first sequence word lines by an enable voltage to conduct the first transistors;

setting the second sequence word line by a disable voltage to isolate the second transistors; and

switching-on the upper switching unit and the lower switching unit for the same column having the selected first transistor, and switching-off the other switching units in the selected memory group.

7. The accessing operation method of claim 6, wherein the enable voltage is a high-level voltage and the disable voltage is a low-level voltage.

8. The accessing operation method of claim 6, further comprising performing a reading operation to read a content stored in a selected second transistor of the second transistors, the reading operation comprising:

selecting a bit line with respect to the selected memory group;

setting a corresponding one of the second sequence word line, which has the selected second transistor, by a constant voltage;

setting the other second sequence word lines by a disable voltage to isolate the second transistors;

setting the first sequence word line by an enable voltage to conduct the first

transistors; and

switching-on one of the upper switching units and one of the lower switching units in different columns, and switching off the other switching units in the selected memory group.

9. The accessing operation method of claim 8, wherein the enable voltage is a high-level voltage and the disable voltage is a low-level voltage.

10. An accessing operation method for the non-volatile memory device as recited in claim 4, comprising performing a programming operation to write a content into a selected first transistor of the first transistors, wherein the programming operation comprising:

selecting a bit line with respect to the selected memory group, wherein the selected bit line is at a voltage used in writing;

setting a corresponding one of the first sequence word line, which has the selected first transistor, by a writing constant voltage;

setting the other first sequence word lines by an enable voltage to conduct the first transistors;

setting the second sequence word line by a disable voltage to isolate the second transistors; and

switching-on one of the upper switching units for a writing period while switching-off the other switching units in the selected memory group.

11. The accessing operation method of claim 10, wherein the enable voltage is a high-level voltage and the disable voltage is a low-level voltage.

12. The accessing operation method of claim 10, wherein the voltage used in writing for the bit line is a low-level voltage or a high-level voltage, and the writing

constant voltage is a very high constant voltage.

13. The accessing operation method of claim 10, further comprising performing a programming operation to write a content into a selected second transistor of the second transistors, wherein the programming operation comprising:

selecting a bit line with respect to the selected memory group, wherein the selected bit line is at a voltage used in writing;

setting a corresponding one of the second sequence word line, which has the selected second transistor, by a writing constant voltage;

setting the other second sequence word lines by a disable voltage to isolate the second transistors;

setting the first sequence word line by an enable voltage to conduct the first transistors; and

switching-on one of the upper switching units for a writing period while switching-off the other switching units in the selected memory group.

14. The accessing operation method of claim 13, wherein the enable voltage is a high-level voltage and the disable voltage is a low-level voltage.

15. The accessing operation method of claim 13, wherein the voltage used in writing for the bit line is a low-level voltage or a high-level voltage, and the writing constant voltage is a very high constant voltage.

16. An accessing operation method for the non-volatile memory device as recited in claim 4, comprising performing an erasing operation to erase contents stored in a memory block unit, wherein the erasing operation comprising:

applying an erasing voltage to all the word lines belonging to the memory block; and

applying a substrate erasing voltage on the memory block unit for an erasing period, wherein the contents of the memory block are erased.

17. A non-volatile memory device, comprising:

a logic input and control unit, receiving a plurality of operation signals;

a control unit, coupled to the logic input and control unit for controlling an operation of the non-volatile memory device;

an address and command register, communicating with the control unit;

a high voltage unit to provide various needed voltages;

a memory cell array unit, which includes the memory array structure of claim 1;

a first direction decoder;

a second direction decoder, wherein the two decoders are coupled with the address and command register, so as to select a memory cell of the memory cell array unit;

a sensing and registering unit to sense and register data; and

an I/O control and buffer unit, used for data transmission of the memory device.

18. A semiconductor memory layout, comprising:

a substrate, wherein a plurality of doped regions are formed in the substrate arranged in a two-dimensional array by rows and columns;

a plurality of isolation structures in the substrate for isolating the doped regions;

an oxide/nitride/oxide (ONO) layer, deposited over a block region of the substrate,;

a plurality of first gate electrodes, located between adjacent two of the doped regions in columns, so as to form a plurality of first transistors;

a plurality of first conductive lines, respectively coupling the gate electrodes of

the first transistors in rows;

a plurality of second gate electrodes, located between adjacent two of the doped regions in rows, so as to form a plurality of second transistors;

a plurality of second conductive lines, respectively coupling the gate electrodes of the second transistors in rows; and

an insulating structure layer, serving isolation function for the first conductive lines and the second conductive lines.

19. The semiconductor memory layout of claim 18, wherein the first conductive lines are even-number word lines and the second conductive lines are odd-number word lines.

20. The semiconductor memory layout of claim 18, wherein the first conductive lines are odd-number word lines and the second conductive lines are even-number word lines.

21. A non-volatile memory array structure, comprising:

a plurality of first transistors, coupled in series to form a plurality of transistor strings in a first direction;

a plurality of second transistors, coupled between adjacent two of the transistor strings, wherein at least a portion of source/drain regions of the first transistor and the second transistor are commonly used;

a plurality of first word lines, respectively coupling gate electrodes of the first transistors in a second direction; and

a plurality of second word lines, respectively coupling gate electrodes of the second transistors in the second direction.